A 400×96 14,467-fps Scan Rate Low Rolling Shutter Distortion CMOS Image Sensor using 12-bit Error-Averaging Column Parallel Pipelined ADC

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ABSTRACT

This paper presents a 12-bit high resolution column parallel pipelined ADC architecture achieving 0.5 µs Analog-to-Digital conversion time, DNL of +0.62 / -0.88 DN, and random noise of 245 µVrms obtained in an ADC TEG chip. We also designed and fabricated a 400 (H) × 96 (V) 8.48 µm pixel pitch CMOS image sensor integrating a revised column parallel ADC and achieved 0.36 µs conversion time, resulting in the maximum scan rate of 14,467 fps. This sensor is suitable for Rolling Shutter Distortion-less imaging and video shooting applications such as machine vision application.

1. INTRODUCTION

Rolling shutter distortion has been steadily improved, especially in high-end large format image sensors, whilst global shutter technology gaining popularity for high-quality video [1-2]. However, it typically trades off dynamic range against increased dark noise. We have been studying a low rolling shutter distortion readout technology to capture natural-look video for fast-moving objects on focal-plane [3]. To do this, high-speed as well as high-resolution column parallel analog-to-digital converters (ADCs) are essential. In this report, we show improvements in scan rate, ADC noise and ADC resolution from our previous sensor [3].

2. ADC ARCHITECTURE

We have been focusing on the pipelined ADC architecture, which enables simultaneous analog-to-digital conversion regardless of ADC resolution. However, conventional pipelined ADCs typically require a large silicon area due to the in-stage capacitors necessary for sampling and Multiplying Digital-to-Analog conversion (MDAC). If the size of capacitors were reduced, the effect of capacitor mismatch causes large differential / integral non-linearity (DNL / INL) due to MDAC gain error, and thermal noise increases due to increased operational amplifier's (OpAmp) bandwidth. To break the trade-off, a capacitor mismatch error averaging (EA) technique was introduced in the past into a 1.5-bit pipelined stages [4-5] to perform an accurate multiply-by-two function without a need of digital calibration or trimming. We adopted this EA technique to our column parallel ADC as shown in Figs. 1 and 2, where 4-capacitor is implemented per stage, instead of normally two. The EA technique is performed in analog domain by interchanging the roles of the capacitors, specifically swapping sampling cap. (C_S) and feedback cap. (C_{FB}) dynamically, during the amplification phase. Multiple residue voltages containing complementary errors are generated, consecutively. These voltages are sampled by succeeding stage capacitors, and the sampled charges are shorted to obtain average voltage. Because the gain errors will be centered around the gain of 2, the averaging operation will cancel the first order capacitor mismatch error as well as the common-mode voltage error [5]. The effect of capacitor mismatch reduction is much more effective than just increasing capacitor size. We verified this technique using MATLAB and found that the technique reduces the DNL and INL roughly by 1/34 and 1/109, respectively as shown in both Fig. 3 and Table I. Also, increasing the number of EA iterations helps clean up ADC performance further including the thermal noise level. According to those simulations, we confirmed that each sampling capacitance (C_S) in Fig. 2 can be significantly reduced to less than 200fF even for targeting 12-bit accuracy.

Figure 4 shows the timing diagram of one ADC conversion, where four samplings during the sampling phase and four combinations of capacitor-sharing or averaging are carried out during the amplification phase, respectively. The control switch signals are intentionally altered such that 4-different amplification patterns are exercised ($C_{FB}/C_S = C_1/C_2$, C_2/C_1, C_3/C_4 and C_4/C_3). The conversion time of the proposed pipelined ADC is 0.5 µs, which is sufficient to suppress rolling shutter distortion in a 4K format [3]. Additionally, to achieve high-speed input response while reducing the transfer gain error, we implemented a symmetrical class-AB differential-pair Flip Voltage Follower (FVF)-based OpAmp [6] with a PMOS Source Follower (SF) to shift a right-half-plane zero generated by the phase compensation capacitor (C_f) to higher frequency region for improved stability, as illustrated in Fig. 5. This OpAmp provides higher DC gain and slew rate than conventional two-stage OpAmp. Furthermore, a Low Pass Filter (LPF) at the output effectively suppresses OpAmp's thermal noise without increasing flicker noise during the amplification phase. This LPF is a first-order type composed of $R_{LPF} = 8.5\text{k}\Omega$ and $C_{LPF} = 780\text{fF}$, which turned out to reduce thermal noise by 47%. We fabricated a test chip, where die micrograph and characterization results are shown in Fig. 6 and Table II, respectively. As predicted in MATLAB simulation, we obtained low readout noise of 245 µVrms and good DNL of +0.62/-0.88 DN in 12-bit resolution. The INL showed much larger than expected due to the parasitic capacitance at the negative input terminal of the OpAmp, indicated as C_P in Fig. 2, which degraded the inter-stage gain. However, we believe that this parasitic capacitance at the critical node can be reduced both by optimizing layout pattern and switched capacitor OpAmp parasitic-insensitive techniques.

3. CIS ARCHITECTURE

We revised aforementioned column parallel pipelined ADC and integrated into a CMOS image sensor, consisting of 3-Tr APS pixel array with an effective pixel count of 400(H) × 96(V), 200 column-parallel 12-bit pipelined ADCs, Vertical Scanning Circuit (VSC), Horizontal Scanning Circuit (HSC), distributed Bias Voltage Generator (Bias), and distributed Clock Generator (Clock Gen) as shown in Fig. 7. The ADC consists of ten 1.5-bit pipelined stages with 2-time EA and 2-bit flash ADC at the end. Each stage outputs 2-bit digital signals, resulting in a total of 22-bit digital outputs reading out from chip to external FPGA. A captured image is reconstructed by applying pipeline ADC's digital error correction on FPGA. To ensure proper bias voltage distribution across the entire ADCs, the bias voltage generators are implemented in distributed structure with each ADC stage. Similarly, to propagate the appropriate clocks across the entire ADC within acceptable inter-stage clock skews, the clock generators, composed of a group of inverters and non-overlap signal generation circuit, are also distributed in parallel along with the stages. Thanks to this implementation, inter-stage sampling timing glitch where amplification phase ends before sampled by succeeding stage can be systematically avoided by distributing the clock from the succeeding stage to preceding stage; from the last stage to the first stage. We adopted a 2-time EA to balance between conversion speed and area constraints while sufficiently reducing rolling shutter distortion and allows for a shorter conversion time than 4-time EA, resulting in 0.36 μs per ADC operation. However, the effects of capacitor mismatch and thermal noise reduction are somewhat diminished. A single ADC is shared between even and odd columns; row time for Digital Correlated Double Sampling (CDS) is twice as the ADC conversion time. The maximum scan rate is 14,467 fps using External CDS, where averaged dark image is stored in FPGA and subtracted as offsets.

4. RESULTS

We designed and fabricated a CMOS image sensor whose die micrograph is shown in Fig.8. This sensor is equipped with a revised 2-time EA column-parallel ADC with 12-bit resolution, 0.36 μs conversion time, the number of effective pixels of 400 (H) × 96 (V), and the maximum scan rate of 14,467 fps using 0.18 μm 1P5M Standard CMOS process, more shown in Table III. Figure 9 shows a captured sample image of the full pixel array under an exposure time of 28 ms with External CDS. From this image, FPNs and random noise are hardly noticeable. Table IV shows the measurement results of FPN and temporal noise in dark conditions in 12 bits when the exposure time and AD conversion time are set to 1.8 ms and 4.8 μs, respectively. Row / Pixel FPNs and temporal noise are prominent. Given that the ADC input range is 1.0V, the temporal noise corresponds to a voltage of 1.14 mVrms. It is significantly affected by the noise superimposed on the reference voltage of the DAC used in each stage of the pipeline ADC. We believe that it is caused by the Low Dropout Regulator (LDO) for reference voltages that is affected by high-frequency noise coming from on-board FPGA where nearly 1GHz of clock frequency is being generated for some reason**.** Therefore, noise countermeasures for the FPGA such as on-chip VREF generation is required as our future work. Regarding Pixel FPN, due to 3-Tr APS pixel where true CDS is not applicable, we believe it would be lowered along with Row FPN.

Figure 10 shows captured sample images of a fast-moving LED light bar with a high scan rate under an exposure time of 70 ms. As shown in Fig. 10(a), when the row time is set to 720 μs for demonstrating purpose, this extended readout duration leads to pronounced rolling shutter distortion. In contrast, as shown in Fig. 10(b), when the row time is set to 0.72 μs, the reduced readout duration mitigates the rolling shutter distortion, making it less noticeable.

5. CONCLUSION

We presented a 12-bit column parallel pipelined ADC consisting of the proposed capacitor mismatch EA techniques, LPF, revised FVF OpAmp and output LPF. The fabricate chip demonstrates the proposed readout scheme maintains high ADC accuracy while significantly reducing rolling shutter distortion; therefore, it is suitable for distortion-less imaging and video shooting applications.

REFERENCE

[1] Richard Butler, *DPReview*, Jan. 4, 2024. [Online] Available at:https://www.dpreview.com/articles/6717086661/sony-a9-iii-image-quality-dynamic-range-analysis [Accessed: Dec. 2024].

[2] Yossy Mendelovich, *Y.M.Cinema Magazine*, Jan. 30, 2024. [Online] Available at: https://ymcinema.com/2024/01/30/ cinema-cameras-with-global-shutter [Accessed: Dec. 2024]

[3] Toshinori Otaka, Shintaro Maekawa et al., *IISW2017,* pp. 316-319, June 2017.

[4] Yun Chiu, *IEEE Trans. on Circuits and Systems*, vol. 47, no. 3, pp. 229-232, March 2000.

[5] M.F. Tompsett, Bang-Sup Song et al., *IEEE Journal of Solid-State circuits*, Vol. 23, no. 6, pp. 1324-1333, 1988.

[6] A. Torralba, R. G. Carvajal, J. Galan and J. Ramirez-Angulo, *ISCAS '03.*, Bangkok, Thailand, pp. 237-240, 2003.

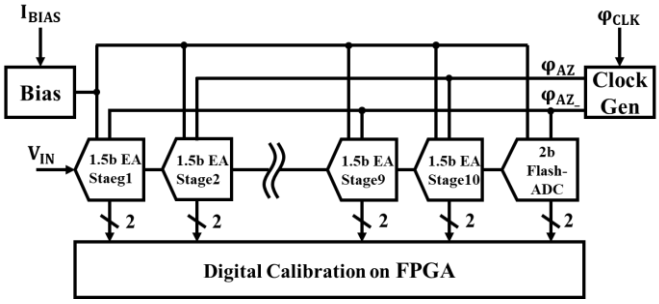


Figure 1. A 12bit pipelined ADC architecture with the capacitor mismatch EA technique.

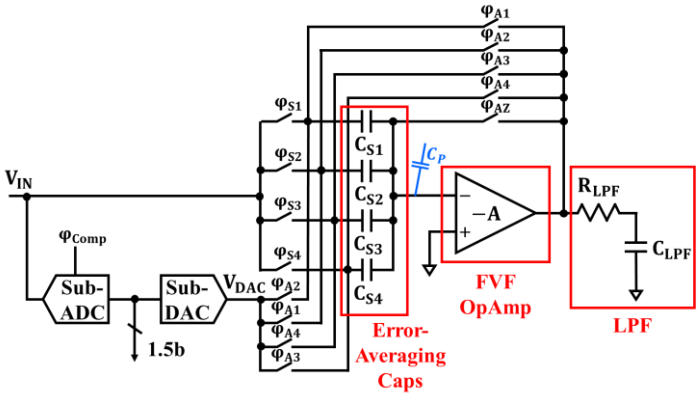


Figure 2. The proposed 1.5bit stage architecture incorporating four in-stage capacitors.

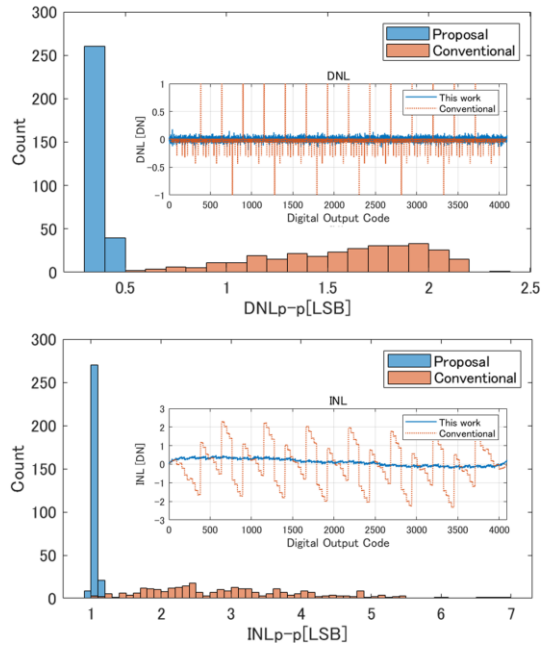


Figure 3. A result of MATLAB mismatch model simulations showing DNL / INL variation histogram of specific input level and as a function of Digital Output Code.

Table I. A result of DNLp-p, INLp-p and random noise of the model simulation.

	DNLp-p [DN]	INLp-p [DN]	Vnoise [DN]
Conventional	1.4146	2.733	0.935
2-time EA	0.041	0.025	0.695
4-time EA	0.037	0.016	0.548

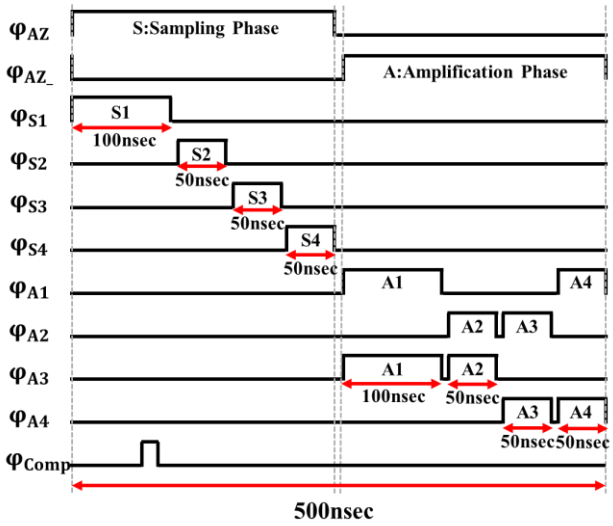


Figure 4. A timing diagram of ADC conversion showing four capacitor combinations in amplification phase.

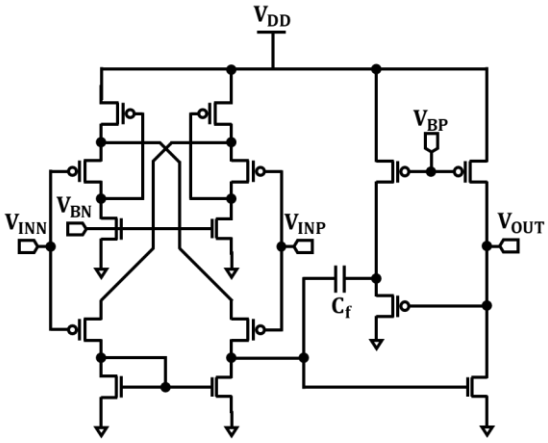


Figure 5. High slew rate Flip Voltage Follower OpAmp with PMOS SF buffer to remove RHP zero.

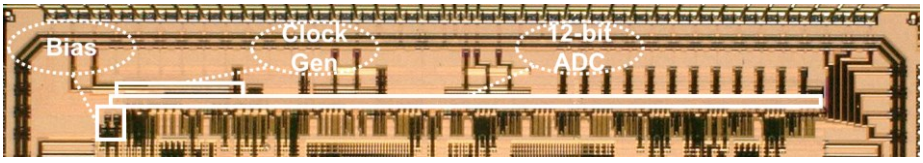


Figure 6. A die micrograph of the ADC TEG chip.

Table II. ADC TEG chip characteristics

Process	0.18 µm 1P5M Standard CMOS
Power Supplies	3.3 V(Analog), 3.3 V(Digital)
ADC Input Range	1.0 V
ADC Pitch	11.54 µm
ADC Area	0.044 mm^2
ADC Conversion Time	0.5 µs
ADC Resolution	12 bits
Random Noise	245 µV,rms
DNL	+0.62 / -0.88 DN
INL	+7.15 / -7.84 DN

Table III. CIS chip characteristics

Process	0.18 µm 1P5M Standard CMOS
CHIP Size	5,180 mm(H) × 5,180 mm(V)
Power Supplies	3.3V(Analog), 4.3V, 3.3V(Digital)
Active Pixels	400 (H) × 96 (V)
Pixel Size	8.48 µm sq.
Row Time	0.72 µs / 1.44 µs *1
ADC Pitch	16.96 µm
ADC Conversion Time	0.36 µs
ADC Resolution	12 bits
Frame Rate	14,467 fps / 7,234 fps*1

*1 Digital CDS

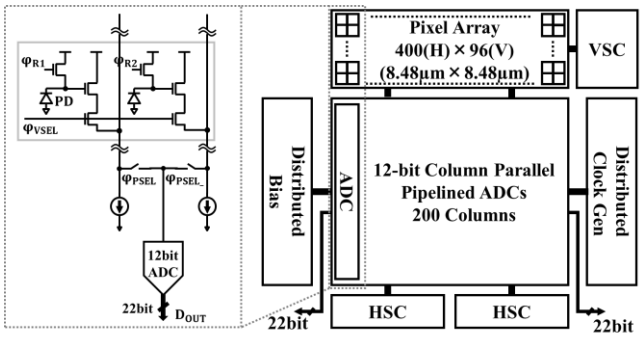


Figure 7. A block diagram of the CIS chip and 3-Tr APS pixel readout slice showing on left.

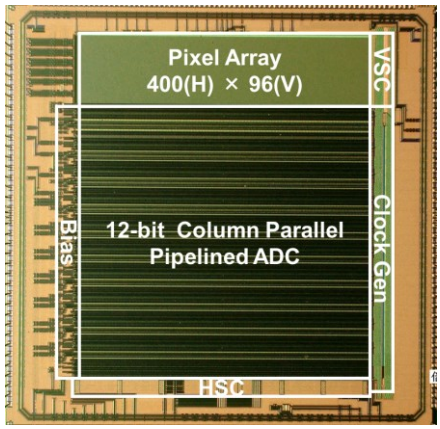


Figure 8. A die micrograph of the CIS chip.

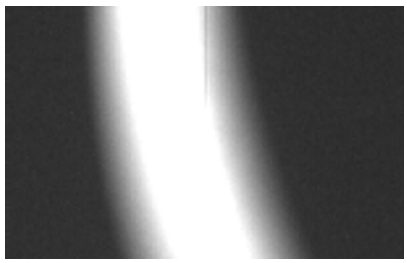
(a) A reference image.

(b) A captured image.

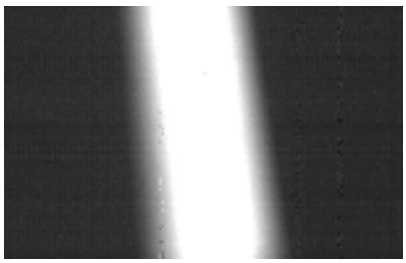
Figure 9. A captured image of Macbeth chart.
(Number of pixels: 400(H) × 96(V), exposure time of 28 ms, External CDS)

Table IV. A measurement result of FPNs and temporal noise in 12 bits

FPN [DN]	1.36
Pixel FPN [DN]	0.95
Column FPN [DN]	0.05
Row FPN [DN]	0.97
Temporal Noise [DN]	4.68



(a) Row time: 720µs.



(b) Row time: 0.72µs.

Figure 10. Captured images of a fast-moving light bar with different scan rates.
(Number of pixels: 152(H) × 96(V), exposure time of 70 ms)